Chip scale package with the chip interconnect Title:

Inventor: Rajendra PENDSE et al. Appln. No. 10/081,491

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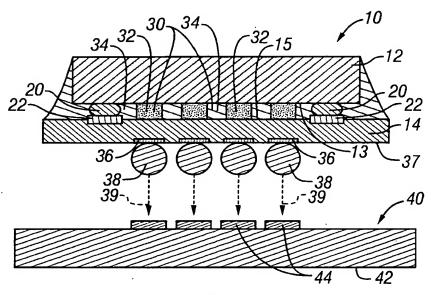


FIG. 1